

## REMARKS

Claims 1-40 were pending in the application. No claims have been amended, canceled or added. Therefore, claims 1-40 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

### Section 103(a) Rejections:

The Examiner rejected claims 1-4, 6-13, 15-25, 27-35 and 37-40 under 35 U.S.C. § 103(a) as being unpatentable over Derrick et al. (U.S. Patent 5,872,980) (hereinafter “Derrick”) in view of Perotto et al. (U.S. Patent 5,630,130) (hereinafter “Perotto”), and claims 5, 14, 26 and 36 as being unpatentable over Perotto as applied to claims 1, 10, 19 and 32 above, in view of AAPA. Applicant respectfully traverses these rejections in light of the following remarks.

Claim 1 of the present application recites, in part, a resource access control mechanism for a multi-thread computing environment operable to manage a **sequence of one or more mutexes associated with a resource**, and, when a requesting thread attempts an access to the resource, to lock a mutex, **to make a determination whether the sequence includes a previous mutex**, and **if a result of the determination is positive, to attempt to lock the previous mutex**.

In rejecting claim 1, the Examiner asserts that Derrick teaches “a sequence of mutexes associated with a resource”, citing col. 7 lines 1 – 2 of Derrick in support. The Examiner’s assertion is incorrect. The cited lines recite “a plurality of semaphores”, but each of these semaphores is for a separate resource, as is clearly evident from col. 6, line 65 – col. 7 line 10 of Derrick:

1. A buffer coupled to a semaphore memory for maintaining data integrity of resources shared by a plurality of devices in a computer system, the semaphore memory containing a plurality of semaphores corresponding to the shared resources, the buffer comprising:

a memory adapted to represent data from at least one of the plurality of semaphores stored in the semaphore memory, the memory comprising a lock and identification field adapted to identify whether the corresponding shared resource is owned by one of the plurality of devices and which of said plurality of devices owns the corresponding shared resource and an address field for relating the lock and identification means to a corresponding one of the plurality of semaphores.

The “semaphore memory” of Derrick contains a plurality of semaphores, but Derrick does not suggest maintaining a sequence of semaphores for any particular shared resource. **Instead, according to Derrick each shared resource of has exactly one associated semaphore, and each semaphore corresponds to exactly one shared resource. The one-to-one relationship between semaphores and resources is repeatedly taught throughout Derrick; see, e.g.,**

When a device needs a shared resource (step 102), it initiates a read to establish ownership of that resource (step 202). While reading for ownership (step 202), the device only locks out accesses by other devices to that same semaphore (step 204). This allows other devices to access other semaphores (and thereby acquire ownership of other shared resources) while the requesting device is acquiring ownership of the requested shared resource. (Derrick, col. 3, lines 55 – 63)

When spin buffer 502 detects the read for ownership, it looks to see if the information corresponding to the semaphore for the shared resource is already within spin buffer 502. (Derrick, col. 5, lines 36 – 39).

3. A buffer, said buffer controlling access to a semaphore memory containing a plurality of semaphores to maintain data integrity of resources shared by a plurality of devices in a computer system, each semaphore corresponding to one of the plurality of shared resources, the buffer comprising: (Derrick; col. 7, lines 24 – 28).

Applicant respectfully submits that neither Derrick nor Perotto, taken singly or in combination, teach or suggest the “sequence of mutexes associated with a resource” recited in claim 1.

Further with respect to claim 1, the Examiner asserts that Derrick teaches “to make a determination whether the sequence includes a previous mutex”, and cites col. 7, lines 36 – 40 of Derrick in support. The Examiner is incorrect. The cited lines of Derrick are reproduced below:

a lock and identification field, said lock and identification field adapted to identify which, if any, of the plurality of devices owns the shared resource corresponding to the semaphore which corresponds to the memory location;

Clearly, there is no suggestion of a sequence of mutexes in the cited lines, much less of “making a determination of whether the sequence includes a previous mutex”, as recited in claim 1.

Still further with respect to claim 1, the Examiner asserts that Derrick teaches “if a result of the determination is positive, to attempt to lock the previous mutex in the sequence, wherein the requesting thread is suspended if the previous mutex is already locked until the previous mutex is unlocked in response to a previous thread finishing access to the resource” at col. 8, lines 24 – 29. The Examiner is mistaken in this interpretation of Derrick as well. The cited lines are:

blocking access by a requesting device to the semaphore corresponding to the one address field which corresponds to the one memory location if the lock and identification data indicate that the requesting device does not own the shared resource and another of the plurality of devices owns the shared resource.

There is no teaching or suggestion in the cited lines, or anywhere else in Derrick or Perotto, of responding to a determination that a sequence of mutexes (of which one mutex has been locked and allocated to a requesting thread) includes a previous mutex by attempting to lock the previous mutex in the sequence.

Applicant respectfully submits that neither Derrick nor Perotto, taken singly or in combination, teach or suggest the combination of limitations recited in claim 1. Accordingly, claim 1 is believed to patentably distinguish over the art cited by the Examiner, and to be in condition for allowance.

Independent claims 10, 19, 22 and 32 each recite limitations using language similar to that of claim 1, and the rejection of these claims is improper for similar reasons as discussed above.

With respect to claim 2, the Examiner asserts that Derrick teaches “on attempting to lock the previous mutex in the sequence when the previous mutex is unlocked, to lock the previous mutex on behalf of the requesting thread and then to unlock the previous mutex on behalf of the requesting thread” at col. 3, line 62 – col. 4, line 9 and col. 8, lines 24 – 30. The Examiner is mistaken. The cited lines of col. 8 are reproduced above. The cited lines in col. 3 of Derrick describe a mechanism of checking to see whether a shared resource is already owned by another device, unlocking accesses to the semaphore and spinning if the shared resource is already owned by another device, and setting a lock bit if the shared resource is not owned by another resource. Neither set of cited lines teach or suggest locking one mutex in a sequence of mutexes associated with a resource on behalf of a requesting thread, and then locking and unlocking a previous mutex within the sequence for the requesting thread, as recited in claim 2. Accordingly, claim 2 is believed to patentably distinguish over the cited art.

With respect to claim 4, the Examiner asserts that Perotto teaches “wherein the mechanism includes an internal mutex operable to protect the locking of the mutex allocated to the requesting thread” at col. 5, lines 9 – 12. Applicant respectfully disagrees. There is no teaching of an additional “internal mutex” to “protect the locking of the mutex” in Perotto; the cited lines merely teach that a bit in a selected data register is set when a shared resource is used by a task, and that the bit is unset when the use of the shared resource by the task ends. Applicant can find no mention of one mutex being used to protect the action of locking another mutex anywhere in Perotto or Derrick. Accordingly, the rejection of claim 4 is further unsupported by the cited art.

In regard to claims 6-9, 15-18, 27-30 and 37-40, Applicant notes that the Examiner repeats his rejection from the previous Office Action in the Final Action, and has not responded to Applicant’s arguments regarding these claims. Applicant respectfully again requests the Examiner to reconsider the rejection of these claims (Applicant’s arguments are repeated here for the Examiner’s convenience). The Examiner states that it would have been obvious to one of ordinary skill in the art to have included an array, a ring buffer, a link list and a circular linked list [in Perotto’s system]

because they would be desirable to perform the customization the most efficient manner possible. Applicant does not understand what the Examiner means by “to perform the customization the most efficient manner possible.” The reason does not appear to have anything to do with using an array, a ring buffer, a link list and a circular linked list to hold a sequence of mutexes. Furthermore, while such data structures may be well known in the prior art **for other purposes**, the prior art does not teach or suggest the use of an array, a ring buffer, a link list or a circular linked list to hold a sequence of mutexes. Moreover, it would not make sense to use such structures in Perotto’s system, or in Derrick’s system, because both Derrick’s and Perotto’s systems only employ a single semaphore per shared resource. The Examiner has not cited any art that teaches or suggests the use of an array, a ring buffer, a link list or a circular linked list to hold a sequence of mutexes for a given resource. Therefore, the rejection of these claims is improper.

**Furthermore, the rejection of claims 5, 14, 26 and 36 as being unpatentable over Perotto in view of AAPA is improper.** As discussed in Applicant’s previous response, Perotto in view of AAPA does not teach or suggest the independent claims from which claims 5, 14, 26 and 36 respectively depend. Therefore, Perotto in view of AAPA also fails to teach or suggest claims 5, 14, 26 and 36. Applicant notes that Derrick was not included in the statement of the rejection of claims 5, 14, 26 and 36. The Examiner has failed to state a *prima facie* rejection of claims 5, 14, 26 and 36.

Applicant also asserts that numerous other ones of the dependent claims recited further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

## CONCLUSION

Applicant submits the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-67700/RCK.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,



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